

## Advanced MMIC T/R Module for 6 to 18 GHz Multifunction Arrays

J. Bugeau, W. Coughlin III, M. Priolo, G. St. Onge\*

Advanced Engineering and Technology Division

Lockheed Sanders, Nashua, NH

### Abstract

A high performance 6-18 GHz dual channel MMIC T/R module is presented with significant advances in integration and performance. This advanced module features critical spacing for 2-dimensional arrays, an Aluminum Silicon Carbide housing, multilayer ceramic substrates for RF and control circuitry, a custom hermetic DC multipin connector, new high performance MMIC LNAs and power amplifiers, and specialized multifunction MMIC chips for a reduced parts count. Each of the two channels feature a selectable horizontal and vertical polarization capability. The module is very densely packaged with 2 complete T/R channels occupying 0.97 in<sup>2</sup>.

### Introduction

Multifunction planar phased arrays that combine broadband ESM and ECM functions into the same steerable array, require state-of-the-art technologies for MMIC circuits, modules, and array integration. A 6-18 GHz dual channel transmit/receive module using many advanced technologies is presented. These advances include MMIC circuit design, dense packaging concepts, and a metal matrix composite package. The implementation of these techniques has resulted in an extremely dense module design with two, dual polarized, 6-18 GHz, T/R channels in a housing size of 4.7"x0.825"x0.25". Previous broadband T/R modules at Lockheed Sanders (1,2) required > 1.0 in<sup>3</sup> for a single channel. The module architecture, key MMIC chips, module control methodology, packaging techniques, and electrical performance are described.

### Module Architecture

The T/R module design is configured for vertical and horizontal polarized planar (2-dimensional) arrays. Either polarization can be selected individually or both can be used simultaneously. The latter allows circular polarization with a slight modification of the module (adding 90° phase shifter circuits). As shown in figure 1, the module block diagram includes two complete T/R channels. This approach was selected based on the critical aperture spacing, and mechanical concerns of a single channel design. Furthermore, the dual channel approach allowed a single digital control circuit to be used for control of both channels.

\* G. St Onge is now with M/A-COM, Lowell MA

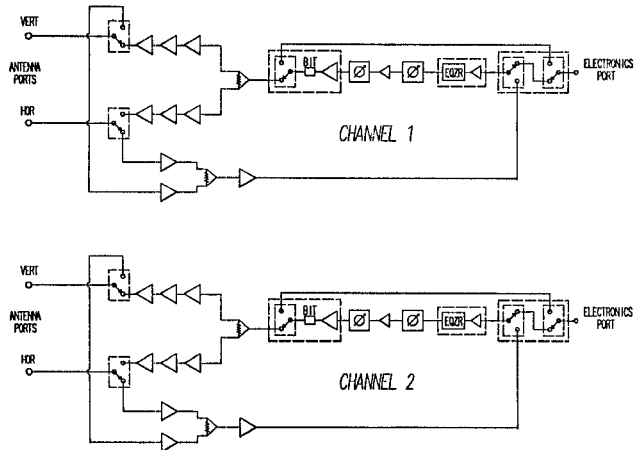


Figure 1. Dual Channel T/R Module Block Diagram

Each channel has a single vector modulator (phase and amplitude control circuit) used in both the transmit and receive states. The vector modulator has 5 bits of phase shift and 4 bits of attenuation control. A built-in-test (bit) detector within the vector modulator checks both transmit and receive paths.

Furthermore, to permit simultaneous vertical and horizontal polarization from each channel, dedicated transmit and receive arms are required. A broadband three section Wilkinson power divider/combiner is used in the transmit and receive paths to perform signal split and sum respectively.

The receive path starts at the antenna port side of the module where the signal passes through a hybrid PIN diode SP2T T/R switch to the low noise amplifiers. The vertical and horizontal paths are combined and a second low noise amplifier provides sufficient gain to offset the losses of the vector modulator. The signal then passes through the vector modulator and out the electronics port. In transmit mode, the signal enters the electronics port, passes through the vector modulator, splits, enters the transmit section where it is amplified to the appropriate levels, and passes through the T/R switch to the antenna port.

### MMIC Chips

The key chip designs are low noise amplifiers (LNA), power amplifiers, and MMICs with high levels of integration (HLI). The low noise amplifier uses a 0.25μm MESFET based on a low noise ion implanted process. A photo of the amplifier and the accompanying data appears in figure 2. The compact size (192 x 122 mils) of the LNA is achieved with a balanced amplifier

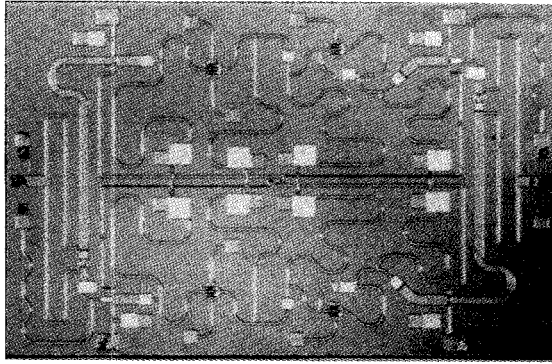


Figure 2. (a) LNA MMIC Chip

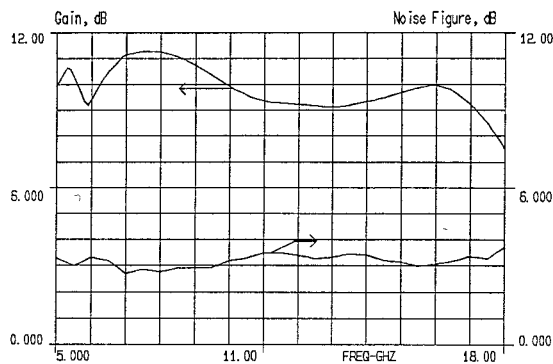


Figure 2. (b) LNA Noise Figure and Gain

topology that uses on-chip couplers to provide an input and output match better than 2.3:1. The LNA uses 300um FET devices resulting in a chip performance of 3.5 dB noise figure and 10 dB of associated gain.

The power amplifier is a two stage balanced design operating over the 6-18 GHz band. It also uses on-chip couplers to provide good input and output matching (better than 2.0:1) in an area measuring only 196 x 117 mils. The output gate periphery totals 3.2mm. Figure 3 shows a photo of the device and the measured power and gain. The output power is greater than 30 dBm over most of the band, the gain is greater than 8 dB, and the power added efficiency is 13.5% minimum.

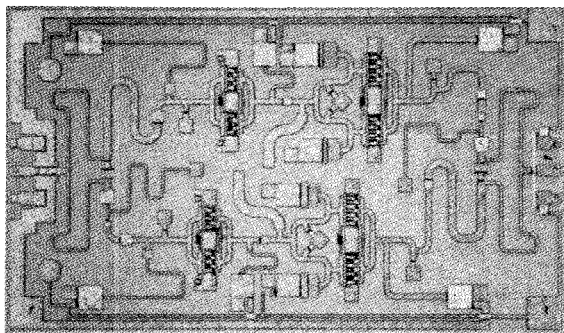


Figure 3. (a) Power MMIC Chip

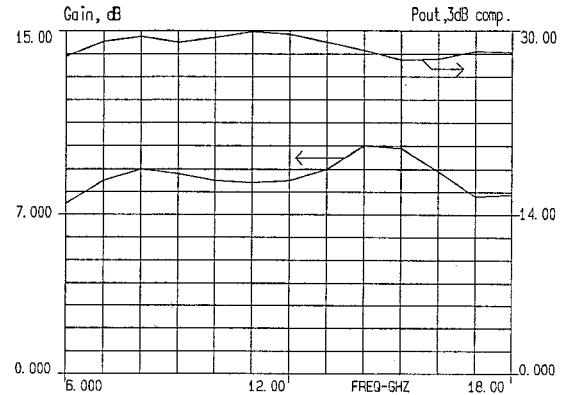


Figure 3. (b) Power and Gain Data

To reduce the number of MMIC circuits in the module, chips with higher levels of integration were used. An example appears in figure 4. The top three circuits are an amplifier, a SP2T switch, and a BIT detector respectively. The chip underneath shows the combination of the three circuits into a larger HLI MMIC. This approach allowed the total number of chips per T/R channel to be reduced from over 30 (1,2) previously to 15. Reducing the number of MMICs per channel permitted the addition of a second channel.

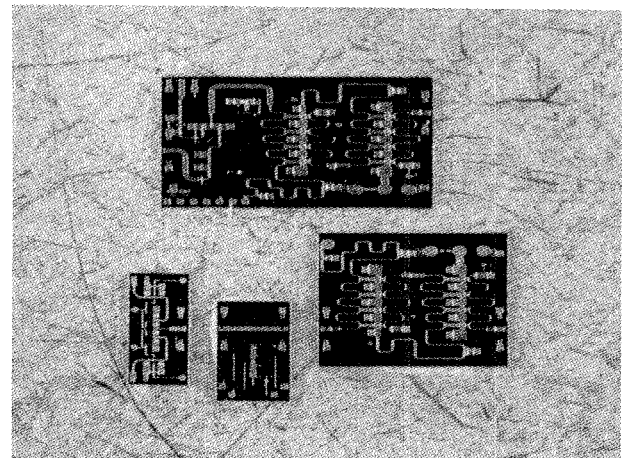


Figure 4. HLI MMIC Photo - 2 Stage Amplifier SP2T Switch, BIT

### Digital Interface Circuit

A digital circuit was designed to control the operation of both T/R channels from a single control board. The design uses a serial to parallel data translation approach to bring the control signals into the module, demultiplex the data, and send it to the phase shifters, attenuators, and T/R switches. This approach reduces the number of control lines. Without the multiplexing, the number of input parallel lines would be 29, but with the serial-to-parallel conversion, the count is reduced to 4 lines. Other circuitry includes TTL level shifters, switches, D/A conversion, and bit selection from either channel. For small size and low noise immunity, a chip and wire construction on a multilayer thickfilm hybrid board was selected.

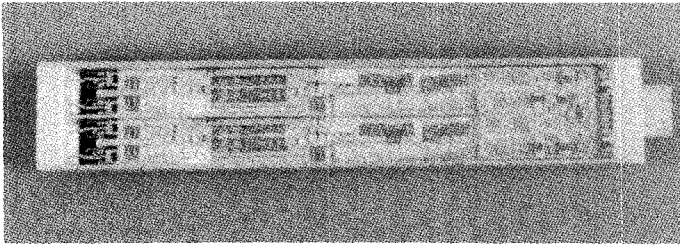


Figure 5. Dual Channel T/R Module

### Mechanical and Packaging Techniques

One key area for the module is packaging. Advanced technologies covering Aluminum Silicon Carbide (AlSiC), multilayer thinfilm RF/DC substrates, and a miniature hermetic DC multipin connector were implemented to minimize module size. Direct die attach and a single sided housing further increased the module's density. The module is shown in figure 5. It measures 4.70"x0.82"x0.25".

The traditional method of microwave module assembly is an aluminum housing (for low weight, good thermal conductivity, availability, and cost) with copper tungsten (CuW) carriers used as a low expansion interface for the MMIC devices. The carriers are attached using screws and other mounting hardware, which consumes considerable volume. This particular housing uses an advanced metal matrix composite (MMC) of AlSiC that combines the advantages of both aluminum and CuW. As shown in table 1, the material is lightweight, has good thermal conductivity, and a coefficient of thermal expansion (CTE) that closely matches GaAs. Furthermore, AlSiC allows the direct attach of carriers and components reducing circuit area. These particular packages were manufactured using the Pressure Infiltration Casting (PIC) process developed by P-Cast Equipment Corporation to produce high quality, net shaped, AlSiC housings. With the PIC process a porous SiC preform is placed in a mold, and infiltrated with a base metal (here aluminum) to a net or near net shape. The T/R housing has .040" walls, .020" septums, a 32uin. surface finish, and Ni/Au plating.

Table 1. Commonly Used Microwave Materials Compared to AlSiC.

Material	CTE ppm/°C	Thermal Conductivity W/m²K	Density g/cc
AlSiC (60%SiC)	8.5	180	2.95
Aluminum (6061)	25.4	180	2.71
CuW (85W/15Cu)	7.0	226	16.4
CuM (80M/20Cu)	7.6	192	9.94
Kovar	5.3	14	8.37
GaAs	5.7		

Multilayer thinfilm substrates were used to rout the RF and DC signals. This thinfilm approach is attractive in this application for both low loss RF lines and tightly spaced (.005" lines, .003" gaps) DC lines. Four different board designs are within the module. A typical board has a .020" thick alumina

base with a sandwiched stripline for RF signal routing. The DC bias and control layers (0.005" thick) are stacked on top with via-holes interconnecting the layers. The boards were fabricated by Holz Industries (3).

A customized hermetic 11 pin DC connector is used to bring control and bias lines into the housing. The connector is very small, hermetic, and has the additional advantage of a one time soldering operation. The RF connectors are Gilbert GPO 2.4mm connectors.

### Performance Results

The measured nominal transmit and receive gains of 20.0 dB are shown in figure 6. The worst case match at either port, for either the transmit or receive state, was a 3.5:1. The noise figure from the module, shown in figure 7, is below 8 dB over most of the band. The nominal output power of the module ranged from 24 to 26 dBm over most of the band from either antenna port. Losses in the switch, and transmission lines, accounted for the drop in power at the module level. A plot of the power is shown in figure 8. The normalized attenuation and phase shift plots are shown in figures 9 and 10. The phase shift over the 10 dB attenuation range is less than 15 degrees (figure 11), while the amplitude variation due to changing phase states is +3/-4 dB (figure 12). The phase and amplitude errors are critical to the performance aspects of an array; they need to be minimal in order to not degrade performance. The isolation between the receive and transmit states is 25 dB minimum. The DC power required for transmit is +12V @ 0.7A, +8V @ 5.5A, and +5V @ 1.8A. This biases up both transmit arms.

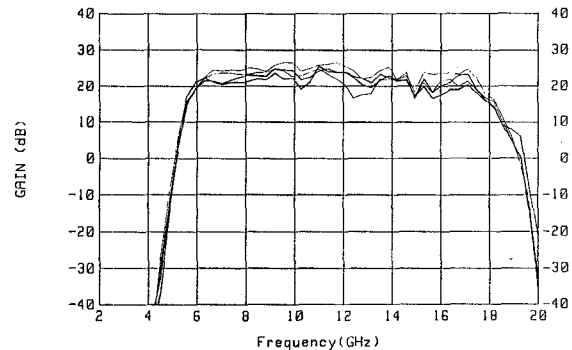


Figure 6. (a) Transmit Gain - All Four Ports

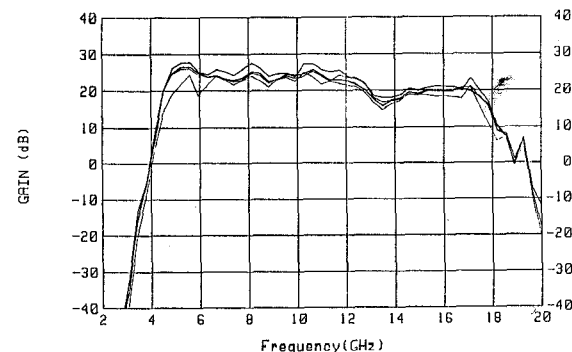


Figure 6. (b) Receive Gain - All Four Ports

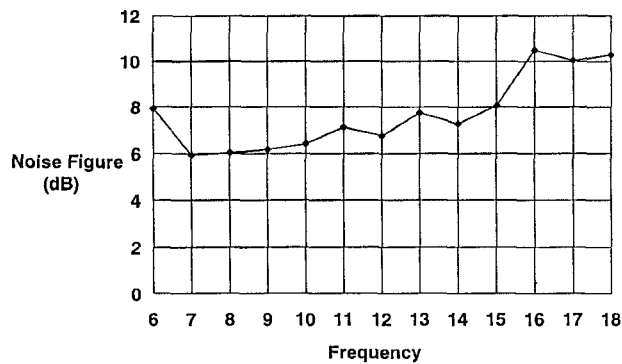


Figure 7. Noise Figure

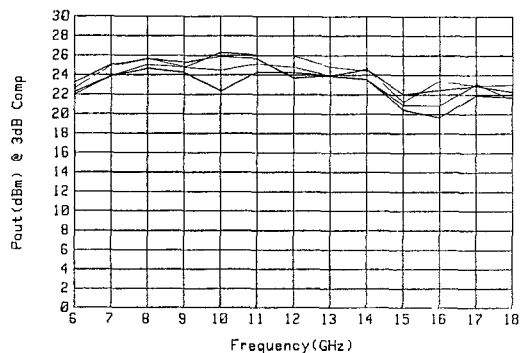


Figure 8. Output Power - All Four Ports

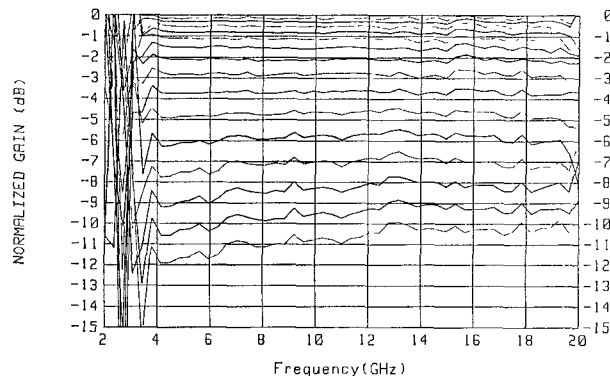


Figure 9. Normalized Attenuation

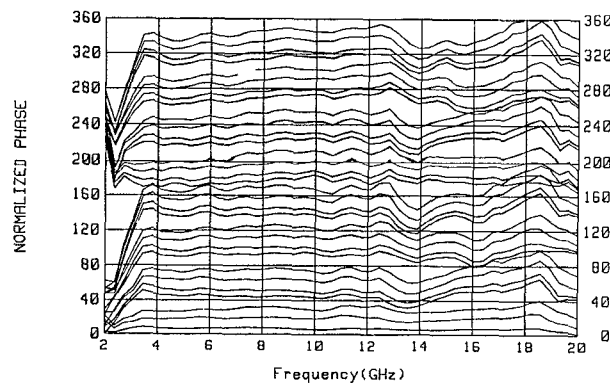


Figure 10. 32 States of Phase Shift

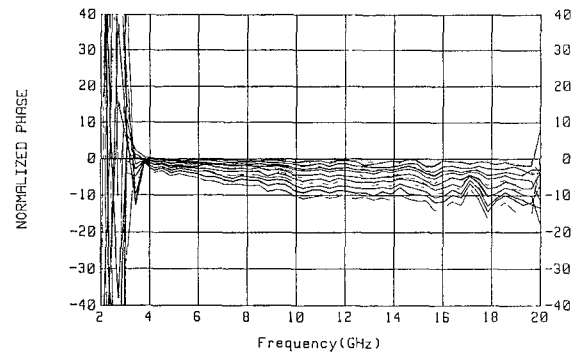


Figure 11. Phase Variation with Changing Attenuation

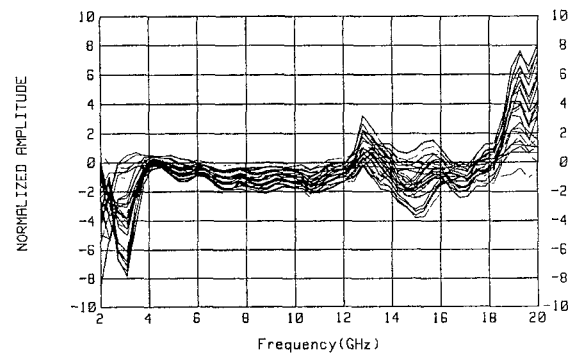


Figure 12. Attenuation Variation with Changing Phase

## Summary

Broadband multifunction active antenna arrays represent an increasingly important requirement for MMIC based T/R modules. A state-of-the-art 6-18 GHz, dual channel, dual polarized MMIC T/R module is presented incorporating advanced MMIC chips and packaging techniques. The module features high performance LNAs, high power amplifiers, HLI MMICs, two channels, dual polarization, an AISiC housing, multilayer thinfilm substrates, and a miniaturized 11 pin hermetic DC connector. A single sided module approach and direct carrier and component attach reduces the module size (to 0.97 in<sup>3</sup>) and enhances manufacturability. The module's nominal noise figure is below 8.0 dB over most of the band, the output power is 26 dBm, and both the measured transmit and receive gains are 20 dB. These advances in module design and packaging are continuing and will make broadband multifunction T/R modules producible and affordable in large quantities.

## Acknowledgements

The authors would like to express their gratitude to Sue Debella, Dave Godbout, Paul Hitchcock, and Risto Laihi for their assistance in the successful development of this module.

References: 1) D. Meharry, et.al., 1989 MTT-S Digest, pp115-118. 2) M. Priolo, et.al., 1990 MTT-S Digest, pp 1227-1230. 3) G. Holz, et.al., 1991 MTT-S Digest, pp 1059-1062.